PCI / PMC / CPCI / PCI-X Bus Analysis

Analyzer

Exerciser

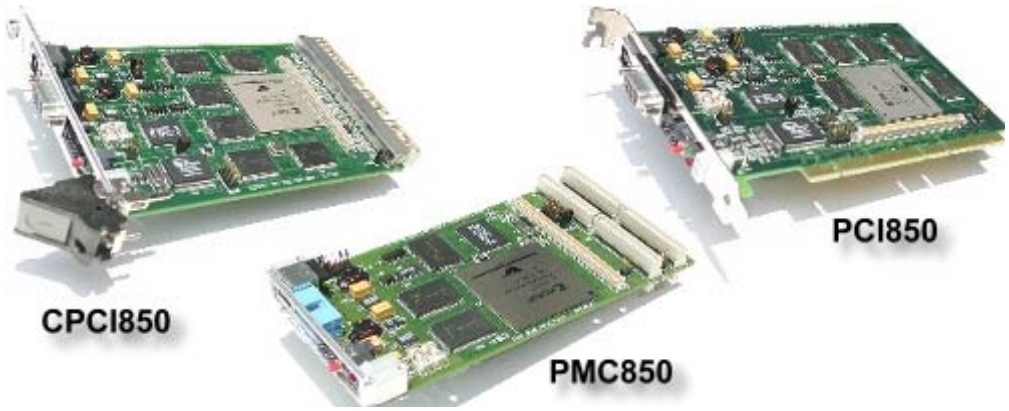
Stimulus

Target

Anomaly

Performance

Compliance



850 System Analyzer/Exerciser

Silicon Control Inc. introduces the ultimate analyzer and exerciser for PCI, PMC and Compact PCI systems. The 850 family of analyzers represent our 3rd generation PCI analyzer combining high performance hardware with a sophisticated and intuitive software interface. The result is a powerful diagnostic tool for bus analysis - all on a single plug-in card.

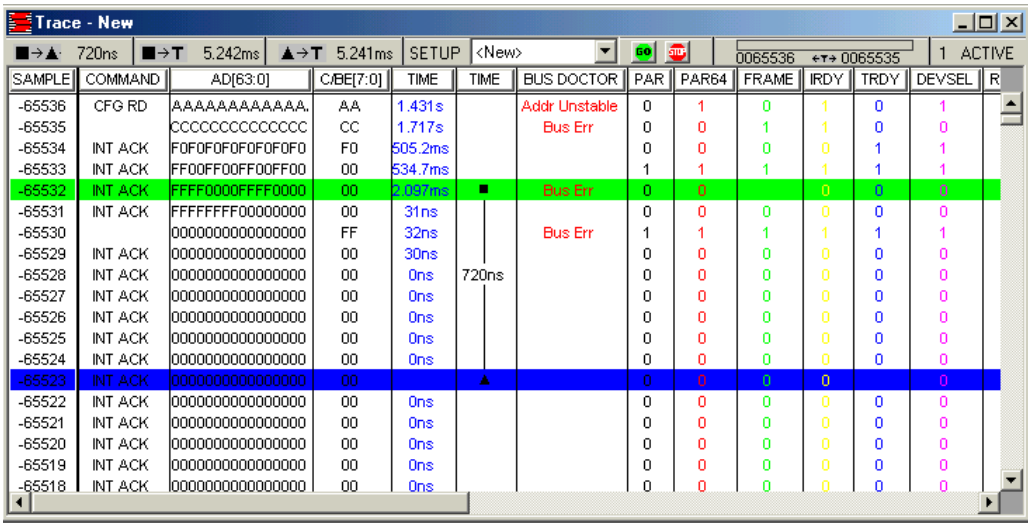
The PCI850 analyzer provides a multitude of functions to help you analyze your system.

- Capturing bus activity using sequential triggers and filters
- Exciser to perform memory, I\O and configuration cycles
- Stimulus generation for hardware simulation
- Target memory with addressable windows
- Anomaly detection of protocol and timing violations
- Performance analysis of utilization, transfer rates, latency, statistics
- Compliance testing

SILICON CONTROL INC.
THE LEADERS IN BUS ANALYSIS
1020 Milwaukee Ave.
Deerfield, Illinois 60015
(847) 215-7947
(847) 808-9090 fax
www.silicon-control.com
info@silicon-control.com

PCI850 State Analysis

State analysis captures bus activity and presents each transaction in an easy to read configur-able display



SAMPLE	COMMAND	AD[63:0]	C/BE[7:0]	TIME	TIME	BUS DOCTOR	PAR	PAR64	FRAME	IRDY	TRDY	DEVSEL	R
-65536	CFG RD	AAAAAAAAAAAAAAAA	AA	1.431s		Addr Unstable	0	1	0	1	0	1	
-65535		CCCCCCCCCCCCCCCC	CC	1.717s		Bus Err	0	0	1	1	0	0	
-65534	INT ACK	F0F0F0F0F0F0F0F0	F0	505.2ms			0	0	0	0	1	1	
-65533	INT ACK	FF00FF00FF00FF00	00	534.7ms			1	1	1	1	1	1	
-65532	INT ACK	FFFF0000FFFF0000	00	2.097ms	■	Bus Err	0	0		0	0	0	
-65531	INT ACK	FFFFFFFF00000000	00	31ns			0	0	0	0	0	0	
-65530		0000000000000000	FF	32ns		Bus Err	1	1	1	1	1	1	
-65529	INT ACK	0000000000000000	00	30ns			0	0	0	0	0	0	
-65528	INT ACK	0000000000000000	00	0ns	720ns		0	0	0	0	0	0	
-65527	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65526	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65525	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65524	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65523	INT ACK	0000000000000000	00		▲		0	0	0	0		0	
-65522	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65521	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65520	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65519	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	
-65518	INT ACK	0000000000000000	00	0ns			0	0	0	0	0	0	

State Display

The state display presents each PCI signal in column form. Signals can be moved, inserted, deleted and color and radix defined. Grouped signals such as address can be collapsed and expanded and their range specified.

Decoded Signals
These predefined signals interpret information on the bus to assist in understanding activity. They are treated like any other signal in the state display.

Defined Signals
These signals or group of signals are defined by the user who assigns a name to a given bus pattern.

Sampling

The PCI850 has 3 basic sampling modes to capture bus activity for state analysis;
CLOCK—every system clock
SYNC—address and data only
TRANSFER—complete cycles

Triggering

Triggers define when the analyzer captures bus activity. Once a trigger is encountered activity can be observed before and after the trigger event. The position of the trigger can be moved within the trace buffer controlling how much data is before or after the trigger event. Triggers can be simple or complex.

Simple trigger
Any PCI signal or combination of signals.

Logically Combined Triggers
Any logical combination of simple triggers using operators such as AND, OR, NOT, Exclusive OR.

Sequential Triggers
This type of trigger is formed by a number of bus events occurring in a specified order. To accomplish this levels are defined. Each active level controls the analyzers operation based on bus events. Jumps to other levels provide complex sequences.

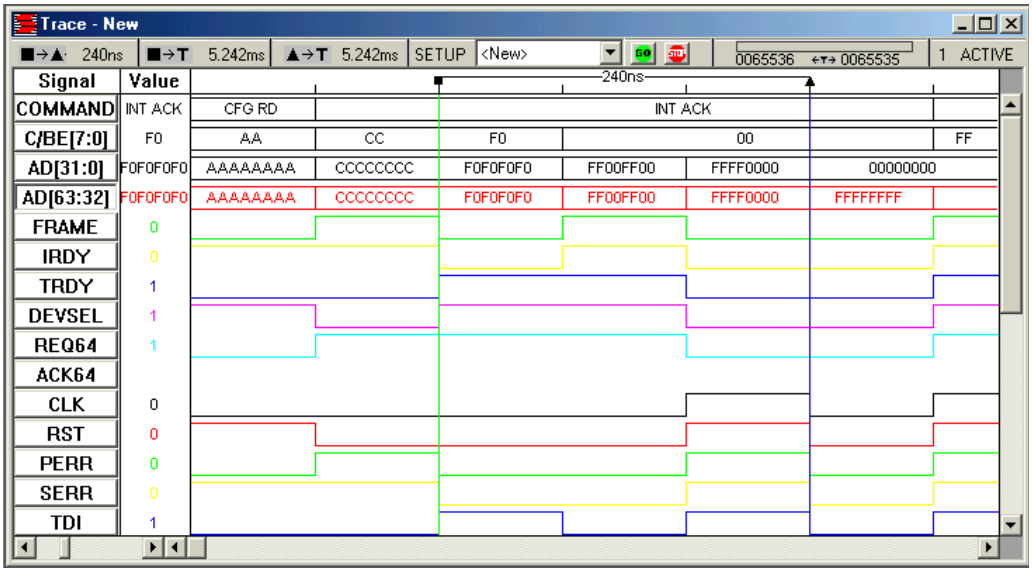
Filtering

Trace filtering defines which events are captured and stored in the analyzers trace buffer. This filtering of data provides only events which are of interest to you.

Silicon Control Inc. 1020 Milwaukee Ave. Deerfield, IL 60015 phone: 847-215-7947 fax:847-808-9090 info@silicon-control.com

PCI850 Timing Analysis

The timing display shows the relation-ship of bus signals and time measure-ments



Timing Display

The timing display represents trace data as waveforms for timing analysis. A numeric value is provided on top of each waveform. As in the state display, signals can be moved, inserted, deleted and color and radix defined. Grouped signals such as address can be collapsed and expanded and their range specified. A zoom is provided to get a better look at waveform relationships.

Sampling

The PCI850 has a precision oscillator used to sample the bus at periodic intervals for timing analysis. The sample rate is selected by the user.

Time Measurements

Cursors can be placed on the timing and state display to measure time between the trigger and a cursor and the time between 2 cursors. Times are shown at the top of the display and in the trace window.

Status Indicators

At the top of the display a status indicator shows the number of samples captured before and after the trigger and the current state of the analyzer.

Capture Control

GO and STOP icons control when tracing starts and halts.

Setup Wizard

To assist in setting up the analyzer for state and timing analysis a Setup Wizard automatically programs the analyzer based on what the user wants to look at. Once a setup is defined it can be saved and later loaded.

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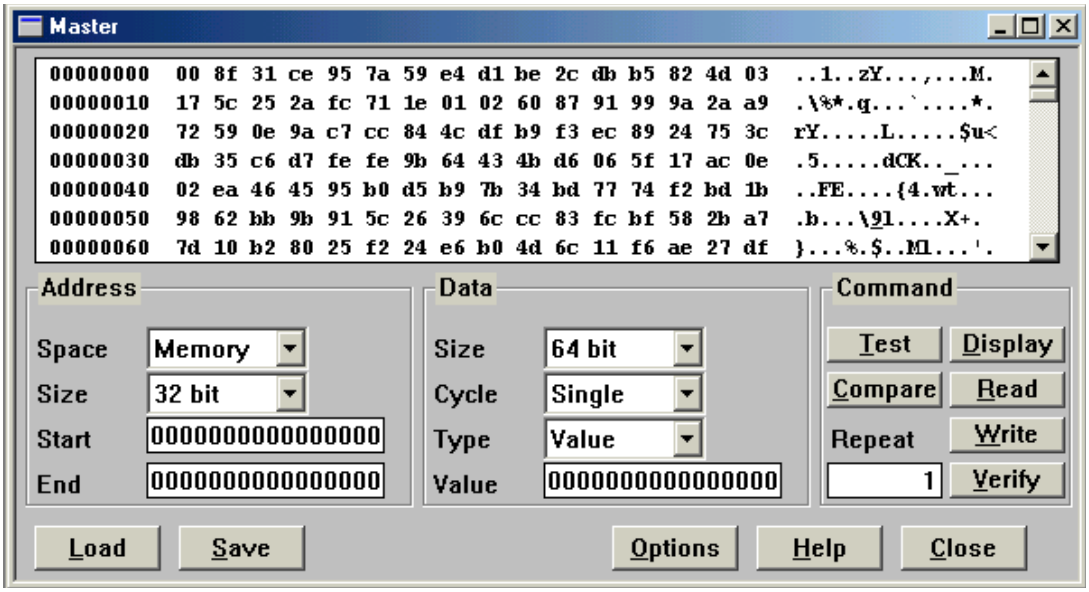
PCI850 Exerciser

The user can initiate memory, I/O and configuration cycles as well as scan configuration space and stimulate the bus



Exerciser

The exerciser performs 3 main functions:

1. Initiator
2. Stimulus Generator
3. Configuration Scan

Initiator

The initiator performs PCI reads and writes to memory, I/O and configuration space. The user has complete control over many aspects of the transfer including:

- Address Space
- Address Width
- Data Width
- Single or Burst
- Write Data Value

The data from a read or write can be obtained from a file or the user. When data is read to the display it is shown in both hex and ASCII. Special tests can be performed including reading and writing test patterns, comparing and verifying data and repeating cycles.

Stimulus

The PCI850 has the ability to generate signal patterns on the PCI bus. These features provide hardware simulation and test system response to events.

Stimulus is driven onto the bus under control of a 16 level sequencer. At each level any combination of bus signals can be specified along with an activation time and wait time synchronized to the system clock. These levels can then be linked together to form complex stimuli. Initiation of this stimulus can be controlled manually or in response to a bus event.

Configuration Scan

An automatic scan of configuration space identifies the boards in a system and displays the configuration information.

A search is performed of all configuration registers and the results are displayed and decoded for easy identification.

The values of the configuration registers are displayed in one window and the decoded meaning in another window.

Vendor names, type of board, version numbers, etc. are displayed for easy interpretation.

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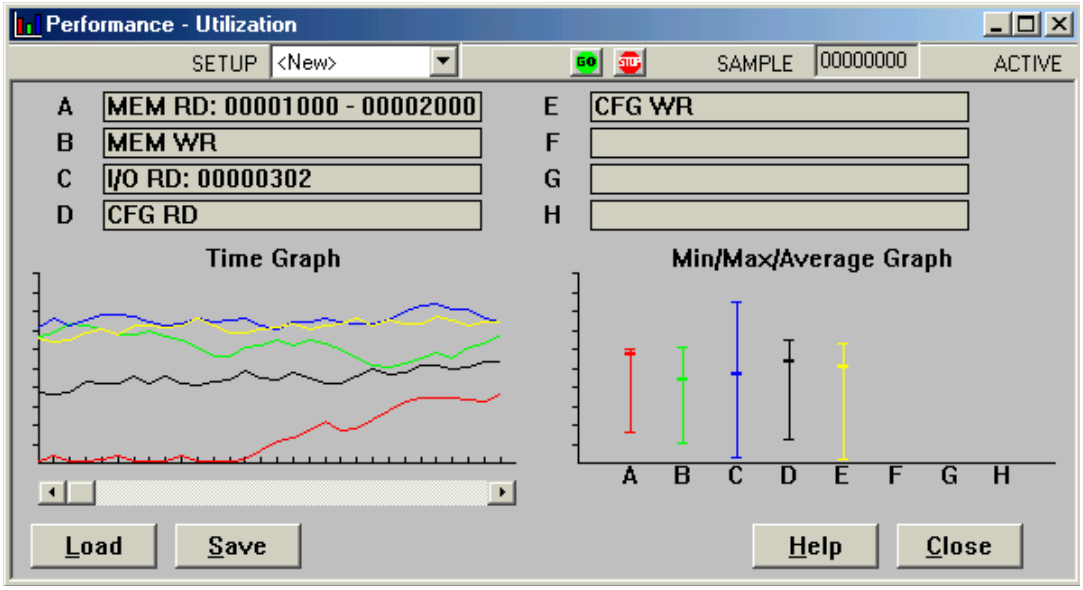
PCI850 Performance

Time graphs and histo-grams give you an over-view of sys-tem perform-ance, bottle-necks and problem areas



There are 5 types of performance measurements that are made in real time with dedicated hard-ware:

- Bus Utilization
- Transfer Rate
- Latency
- Burst Distribution
- Statistics

Bus Utilization

This measurement identifies the resources that are using the bus. These can include address usage, command type and overall idle and busy times.

Transfer Rate

The transfer rate measurement measures in MB/s the speed of data transfers. These measure-ments can be specified for spe-cific address ranges and cycles.

Latency

The efficiency of data transfers in a system depend upon the laten-cies involved. Measurements are taken of master, target, address, data and arbitration to provide a look at latencies that slow a bus down.

Burst Distribution

The amount of data transferred during each cycle is measured and displayed in 8 ranges. The ranges include single byte transfers and up.

Statistics

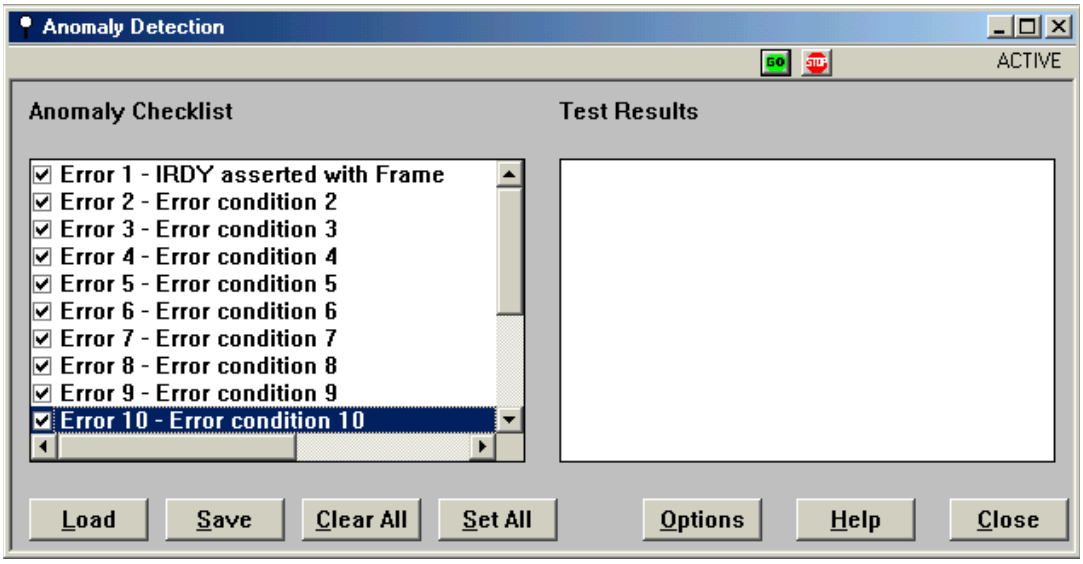
Statistics can be obtained for any bus signal or group of signals. For example the number of memory reads, memory writes, writes to an address or address range can be counted.

Performance Display

The performance display consists of a moving time graph and an average/min/max bar or pie chart. The time graph shows the current measurement and is updated at fixed time intervals specified by the user. The bar chart averages this moving data and tracks the min and max values. A scroll bar under the time graph lets you re-view the previous data.

PCI850 Anomaly Detection

Protocol and timing violations are automatically detected and displayed



Automatic Anomaly Detection

The PCI850 continuously monitors and detects over 100 protocol and timing violations. Dedicated hardware checks setup and hold times, unstable signals and glitches on lines. Protocol checking screens for illegal signal assertions referenced to the PCI specification.

Anomaly Display

The anomaly display is divided into 2 windows;

1. Anomaly Checklist
2. Test Results

Anomaly Checklist
The anomaly checklist window allows selection of specific tests. Set All and Clear All buttons are provided to select all the tests and clear all the tests. The checklist can be saved and later loaded.

Test Result Window
After starting the anomaly test the result window displays all violations detected. The user can scroll through these results as well as save them to a file.

State/Timing Display

During state and timing analysis violations are stored in the trace buffer as selected in the checklist. A description of the violation can be selected for display in the state and timing windows.

To include this information in a state or timing display simply select the Bus Wizard decoded signal. The Bus Wizard displays a short description of the error. Highlighting the error displays a complete description of the anomaly.

Trigger and Filter Setup

Any anomaly can be selected as a trigger or filter when tracing bus activity. When used as a trigger this provides a view of activity that lead up to the error. Selecting anomalies for a filter allows the user to trace only errors detected by the anomaly checker.

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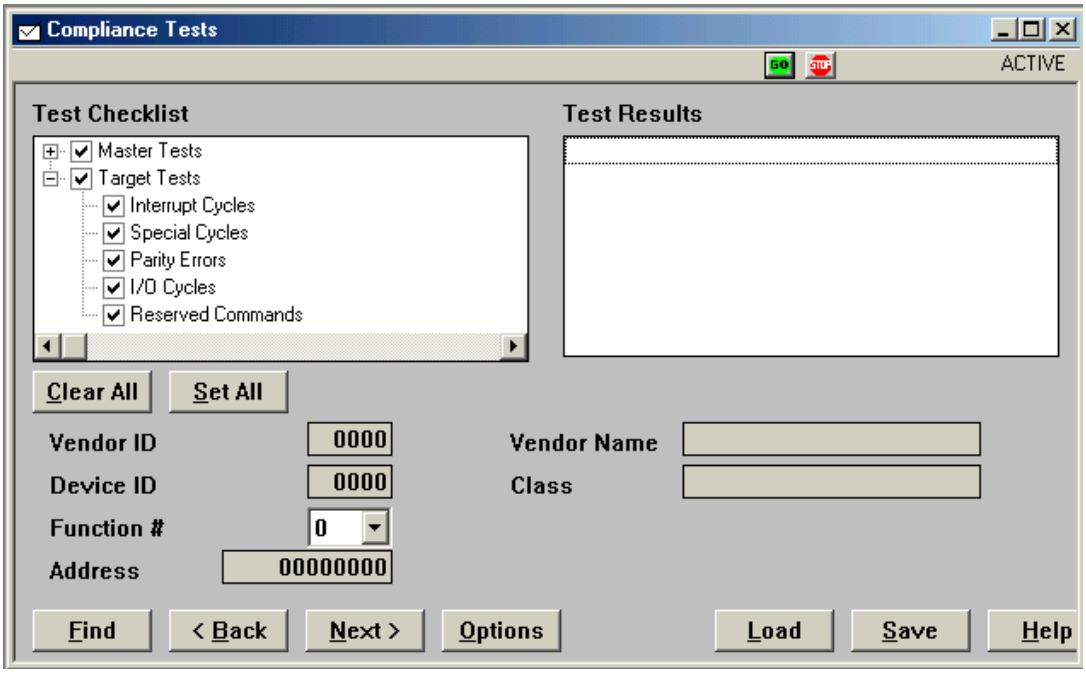
PCI850 Compliance Testing

Testing against a compliance checklist is performed to insure PCI compatibility



Compliance Testing

Compliance testing is performed based on the PCISIG compliance checklist. A complete suite of master and target tests are performed automatically. During some tests the user is prompted to change the system setup or initiate a bus cycle from the device under test.

Compliance Display

The compliance display is divided into 2 windows;

1. Test Checklist
2. Test Results

Test Checklist
The compliance test checklist window allows selection of specific tests. Set All and Clear All buttons are provided to select all the tests and clear all the tests. Tests are grouped in categories for easy group selection. The checklist can be saved and later loaded.

Test Result Window
After starting the compliance test the result window displays each test and if the test passed. The user can scroll through these results as well as save them to a file.

Device Identification

Before starting the compliance test the configuration space is scanned to determine the device to be tested. Vendor information is displayed to identify the device. To select another device Back and Next buttons start a new scan of the configuration space before and after the current device.

Multiple Test Functions

Many of the features of the PCI850 are used during the compliance tests. These include tracing, exercising, anomaly detection, target access and configuration scanning.

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PCI850 Other Features

Target Memory

A target memory is provided which is accessible through the PCI bus. An address window can be defined for PCI transfers. The contents of the target memory can be displayed and altered directly by the user or through a file. Data in the target memory can be used for exerciser functions. For example data written into the target memory can be sent back on the bus in it's original state or modified.

Configuration Scan

The configuration scan automatically detects devices on the bus and displays configuration information in 2 windows:

1. Block configuration data displays the configuration information in binary form.
2. Decoded Configuration interprets the information and displays Vendor name, class description, revision codes, etc.

To select another device Back and Next buttons start a new scan of the configuration space before and after the current device.

Configuration information can be saved, printed and loaded back for display.

External Trigger Inputs

Eight external inputs are provided for monitoring signals external to the PCI connector. These signals can be selected for display in the state and timing windows and used in trigger and trace setups.

A trigger cable is included which plugs into a trigger connector on the front panel. This connector also provides a ground signal.

External Trigger Output

One trigger output is provided to facilitate the triggering of other test equipment. When a trigger is encountered this output is driven active. The polarity and duration of the trigger output is specified by the user. This signal is available on the same front panel trigger connector along with the trigger inputs.

Communication Interfaces

The PCI850 communicates with a PC or terminal through an RS232 or USB interface. The RS232 interface operates at speeds up to 115K baud and the USB interface at 12Mbits/sec. All setup and display results are sent over these interfaces. USB (type B) and RS232 (DB9) connectors are located on the front panel.

External Power

The PCI850 can be powered by an external power supply. This feature can be useful when monitoring a system power up sequence. A power connector is located on the front panel. This connector supplies power to the analyzer and is fuse protected. A power cable is included with the analyzer.

Expansion Connector

A 200 pin expansion connector is located on the analyzer for optional plug on accessories. These include board test adapters and a 533 Mhz high speed timing module.

Reset Options

A pushbutton reset switch and reset jumpers select options for resetting the board and system.

LED Indicators

A green LED illuminates after the analyzer has passed it's self test and a red LED is under user control.

Reprogramability

New firmware updates can be downloaded into flash memory on the analyzer. Updates are available on our Web site.

PCI850 Specifications

General Specifications

PCI Compliance:	PCI 2.2 , PCI-X 1.0 Compliant
Bus Size:	64 or 32 bit
Bus Signal Levels:	5V or 3.3V

Trace Specifications

Trace Memory:

PCI850-1	128K by 144 bits
PCI850-2	256K by 144 bits
PCI850-3	512K by 144 bits
PCI850-4	1M by 144 bits
PCI850-5	2M by 144 bits

Sampling Rate:	133 Mhz
High speed module	533 Mhz
Sampling Modes:	System Clock System Clock w/ Address/Data System Clock w/ Transfers On board precision Oscillator (7.5ns to 15us)
Sampled Signals:	AD[63:0], C/BE[7:0], FRAME, DEVSEL, TRDY, IRDY, PAR, REQ, GNT, RST, LOCK, CLK, INTA, INTB, INTC, INTD, PAR64, PERR, SERR, REQ64, ACK64, TDO, TDI, TCK, TMS, TRST, SDONE, SBO, EXT[7:0]
External Inputs:	8 Front Panel Trace/Trigger
External Outputs:	1 Programmable Trigger Output
Triggers:	8 Trigger Conditions each specifying 100 PCI signals, 8 external triggers and anomaly errors
Trigger Types:	Single Condition Logical Combination 16 Level Sequencer
Trigger Positions:	0%, 25%, 50%, 75%, 100%
Occurrence Counters:	16 hardware counters 20 bits
Event Counters:	16 hardware counters 20 bits
Time Tag:	7.5 ns to 60 sec.

Exerciser Specifications

Initiator Bandwidth:	528 MB/s rate
Initiator Bus Width:	64 or 32 bit
Initiator Transfers:	Memory, I/O, Configuration

Target Specifications

Target Memory:

PCI850-1	1 MB
PCI850-2	2 MB
PCI850-3	4 MB
PCI850-4	8 MB
PCI850-5	16 MB

Target Bandwidth:	528 MB/s burst rate
Target Bus Width:	64 or 32 bit

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PCI850 Specifications

Protocol Violations Checked

Master

1 FRAME deasserted before IRDY asserted
2 FRAME asserted without IRDY or TRDY
3 FRAME not deasserted within 3 clocks after STOP
4 No FRAME within 16 clocks from GNT
5 No IRDY within 8 clocks from FRAME
6 No TRDY or STOP within 16 clocks from initial data phase
7 No TRDY within 8 clocks after initial data phase
8 No IRDY after FRAME asserted
9 DEVSEL deassserted before tranasction complete
10 Invalid Command on CB/E[3:0]
11 Invalid Command on CB/E[7:4] during DAC cycle
12 IRDY asserted during turnaround cycle
13 Address PAR error
14 Data PAR error
15 Address PAR64 error
16 Data PAR64 error
17 No PERR after parity error
18 Improper Master Abort - IRDY deasserted before TRDY/STOP asserted
19 FRAME asserted before GNT
20 STOP not deasserted after FRAME deasserted
21 FRAME and IRDY high when STOP is asserted
22 STOP not asserted when FRAME asserted

Target

23 No target turnaround
24 Lock not released
25 STOP deasserted with FRAME deasserted
26 PERR asserted during special cycle
27 PERR asserted during address cycle
28 TRDY asserted during target abort
29 LOCK asserted after target abort
30 IRDY asserted when FRAME deasserted
31 TRDY asserted before DEVSEL
32 IRDY asserted before DEVSEL
33 STOP asserted before DEVSEL
34 LOCK asserted during address phase

General

35 Maximum write completion time exceeded
36 REQ to GNT time > 15 clocks
37 REQ to GNT time > 30 clocks
38 REQ to GNT time > 45 clocks
39 REQ to GNT time > 60 clocks
40 REQ to GNT time > 90 clocks
41 Improper fast back-back cycle
42 AD[1:0] not 0 during MWI cycle
43 REQ64 not asserted with FRAME
44 ACK64 not asserted with DEVSEL
45 Master Abort during DEVSEL
46 FRAME deasserted after DAC cycle
47 Target responding to invalid command
48 Target response before DEVSEL
49 Address does not match Byte Enables

Timing Violations Checked

Unstable Signals

50 AD[7:0] Unstable during address phase
51 AD[15:8] Unstable during address phase
52 AD[23:16] Unstable during address phase
53 AD[31:24] Unstable during address phase
54 AD[39:32] Unstable during address phase
55 AD[47:40] Unstable during address phase
56 AD[55:48] Unstable during address phase
57 AD[63:56] Unstable during address phase
58 AD[7:0] Unstable during data phase
59 AD[15:8] Unstable during data phase
60 AD[23:16] Unstable during data phase
61 AD[31:24] Unstable during data phase
62 AD[39:32] Unstable during data phase
63 AD[47:40] Unstable during data phase

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PCI850 Specifications

64 AD[55:48] Unstable during data phase
65 AD[63:56] Unstable during data phase
66 CBE[3:0] Unstable during address phase
67 CBE[7:4] Unstable during address phase
68 CBE[3:0] Unstable during data phase
69 CBE[7:4] Unstable during data phase

Setup and Hold

70 AD[7:0] not valid within 12ns of clock
71 AD[15:8] not valid within 12ns of clock
72 AD[23:16] not valid within 12ns of clock
73 AD[31:24] not valid within 12ns of clock
74 AD[39:32] not valid within 12ns of clock
75 AD[47:40] not valid within 12ns of clock
76 AD[55:48] not valid within 12ns of clock
77 AD[63:56] not valid within 12ns of clock
78 CBE[3:0] not valid within 12ns of clock
79 CBE[7:4] not valid within 12ns of clock
80 DEVSEL not valid within 12ns of clock
81 FRAME not valid within 12ns of clock
82 IRDY not valid within 12ns of clock
83 TRDY not valid within 12ns of clock
84 LOCK not valid within 12ns of clock
85 STOP not valid within 12ns of clock
86 REQ64 not valid within 12ns of clock
87 ACK64 not valid within 12ns of clock
88 PERR not valid within 12ns of clock
89 PAR not valid within 12ns of clock
90 PAR64 not valid within 12ns of clock

General

91 CLK Period < 15ns (66 Mhz system)
92 CLK Period < 30ns (33 Mhz system)
93 CLK High < 6ns (66 Mhz system)
94 CLK Low < 6ns (66 Mhz system)
95 CLK High < 11ns (33 Mhz system)
96 CLK Low < 11ns (33 Mhz system)
97 Gliches on CLK
98 RESET high to first Configuration access invalid
99 RESET high to first FRAME active invalid
100 RESET to REQ64 time invalid
101 Gliches on RESET

Performance Analysis

Functions:
- Bus Utilization
- Transfer Rate
- Latency
- Burst Distribution
- Statistics

Measurement Displays:
- Moving Time Graph
- Average Bar Chart
- Minimum Bar Chart
- Maximum Bar Chart

Number of Measurements:
- 8 Simultaneous Conditions

Measurement Conditions:
- All Bus Signals
- Commands
- Address Ranges
- Initiator Specific
- Target Specific
- Arbitration Specific

Compliance Testing

Test Conditions: PCISIG Checklist

Test Type: Automatic/Manual

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PCI850 Specifications

Front Panel Interfaces

RS232 Port: DB9 connector, 110 to 115K Baud (cable included)

USB Port: Series B connector, 12 MB/s (cable included)

Indicators: GO LED, User LED

Pushbutton: Reset Analyzer or System

External Power: 2 Conductor front panel (cable included)

Trigger: 10 pin socket (8 in, 1 out, 1 ground) (cable included)

Fuses: Main power and External power

Power Requirements

Operating—5V at 3 amps max
Standby—5V at 1 Amp max
Generated on-board– 3.3V and 2.5V

Dimensions:

PCI850—PCI Short Card
PMC850– Single slot PMC card
CPCI850– 3U Compact PCI card

Parhelia B.V.
info@parhelia-bv.eu
www.parhelia-bv.com
✆+31(0)10 741 00 28

Ordering Information:

PCI Analyzers

PCI850-1	128K Sample Trace Buffer 1 MB Target Memory
PCI850-2	256K Sample Trace Buffer 2 MB Target Memory
PCI850-3	512K Sample Trace Buffer 4 MB Target Memory
PCI850-4	1 M Sample Trace Buffer 8 MB Target Memory
PCI850-5	2 M Sample Trace Buffer 16 MB Target Memory

Compact PCI Analyzers

CPCI850-1	128K Sample Trace Buffer 1 MB Target Memory
CPCI850-2	256K Sample Trace Buffer 2 MB Target Memory
CPCI850-3	512K Sample Trace Buffer 4 MB Target Memory
CPCI850-4	1 M Sample Trace Buffer 8 MB Target Memory
CPCI850-5	2 M Sample Trace Buffer 16 MB Target Memory

PMC Analyzers

PMC850-1	128K Sample Trace Buffer 1 MB Target Memory
PMC850-2	256K Sample Trace Buffer 2 MB Target Memory
PMC850-3	512K Sample Trace Buffer 4 MB Target Memory
PMC850-4	1 M Sample Trace Buffer 8 MB Target Memory
PMC850-5	2 M Sample Trace Buffer 16 MB Target Memory

All analyzers include Windows and API software, cables, carrying case and manuals.