PCIe8g3 S5-40G

PCIe Gen3 x8 board with Stratix V FPGA, 40G QSFP+, and 10G SFP/+s

Includes active FPGA heat sink (not shown).

Description

The PCIe8g3 S5-40G is a fast, versatile PCI Express (PCIe, Gen3) x8 interface with one 40G QSFP+ and up to two 10G SFP/+ ports. It supports 1/10/40GbE, OC3/12/48/192 (STM1/4/16/64), or OTU1/2/2e/2f.

Each port links to the FPGA for serialization / deserialization (SERDES) and clock recovery. Each port has its own reference clock, programmable for 10–210 MHz.

The single FPGA is an Altera Stratix V GX (A3, A5, A7, or A9) with access to two independent 4 GB blocks of DRAM (DDR3), which can act as data buffers. The FPGA provides up to 16 independent DMA channels via EDT FPGA configuration files.

A time code input (1 pps or IRIG-B) also is included, with an option for either DB9 or BNC cabling.

EDT FPGA configuration files are included to support 1GbE and 10GbE at the PHY layer; OC3/12/48/192 and OTU1/2/2e/2f (raw, framed, framed and descrambled); and demultiplexing. Custom files can be requested.

Features

- PCIe (Gen3) x8 interface with one 40G QSFP+ and up to two 10G SFP/+s
- Data formats: 1/10/40GbE, OC3/12/48/192 (STM1/4/16/64), OTU1/2/2e/2f
- FPGA + DMA: One user-programmable Altera Stratix V 5SGX (A3, A5, A7, or A9), configurable for up to 16 independent DMA channels
- DRAM (DDR3): Two independent 4 GB blocks
- EDT intellectual property for 10GbE PCS and PMA layers, SONET/SDH framing, demultiplexing, and G.709 framing
- Time code input: 1 pps or IRIG-B, with user-configurable output

Applications

- Telecommunications monitoring, recording, and processing
- SONET/SDH to ethernet conversion
- Multiple other network processing applications

Specifications

Product Type	PCIeGen3 x8 board with Stratix V FPGA, 40G QSFP+, and up to two 10G SFP/+s for up to 40GbE / OC192 (STM64) / OTU2f.
FPGA Resources + DMA	One programmable FPGA (Altera Stratix V GX (A3, A5, A7, or A9), user-configurable for up to 16 independent DMA channels
Memory	DRAM (DDR3), two independent 64-bit wide 4 GB blocks for snapshot recording / data buffering
Clocks (Reference)	Up to four (one per port), each independently programmable from 10 to 210 MHz with limited support for reference loop timing.
Data Rates	Dependent on such factors as data format and system variables.
Data Format (I/O)	Via multiple ports, the board supports various data formats as shown below: 1/10/40GbE, OC3/12/48/192 (STM1/4/16/64), OTU1/2/2e/2f). Also provided is a time code input (to connect to an external source) for 1 pps, IRIG-B, or other input, with user-configurable output.
Transceivers	The board has multiple transceiver options, as shown below.

Up to two SFP/+*	**ELECTRICAL (1GbE)**	**OPTICAL (10GbE) SFP/+* 1550 nm**	**SFP/+* 1310 nm**	**SFP/+* 850 nm**
Output power (dBm)	–	–2 to +3 / 0 to +4	–9.5 to –3 / –8.2 to +0.5	–9 to –2.5 / –5 to –1
Center wavelength (nm)	–	1500–1580 / 1530–1565	1270–1360 / 1260–1355	830–860 / 840–860
Sensitivity (dBm)	–	–28 / –23	–18 / –10.3	–18 / –7.5
Maximum input power (dBm)	–	–9 / –7	0 / +0.5	0 / +0.5
Connector	RJ45 transceiver	LC	LC	LC

* An **SFP** at 1550, 1310, or 850 nm can support 1GbE, OC3/12/48 (STM1/4/16), or OTU1.
An **SFP+** at 1550 or 1310 nm can support 10GbE, OC192 (STM64), or OTU2/2e/2f — or, at 850 nm, 10GbE only.

Up to one QSFP+	**ELECTRICAL**	**OPTICAL (40GbE) QSFP+ 850 nm**
Output power (dBm)	–	–7.6 to –1.0
Center wavelength (nm)	–	840–860
Sensitivity (dBm)	–	–5.4
Max. input power (dBm)	–	+3.4
Connector	–	1x12 MPO

Cooling	Active heat sink	
Connectors	One 7-pin Lemo for time code input One RJ45 or LC on each SFP/+ as shown above One MPO on QSFP+	
Cabling	To 7-pin Lemo on board, from time code source For other cabling, consult EDT for purchase options.	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)
Physical	Weight Dimensions	8.5 oz. (with active heat sink, but without transceivers) 6.6 x 4.2 x 0.75
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)	0° to 40° C / -40° to 70° C 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	System must have a PCI Express bus (8 or 16 lanes) that is not dedicated to display use only. Software is included for Windows and Linux; for versions, see www.edt.com.	

Ordering Options

- FPGA: A3 / A5 / A7 / A9
- Transceivers: [options above]
- Cabling (for time code input): DB9 / BNC

Bold is default. For more options, see main board detail. **Ask** about custom options.